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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,686	01/05/2004	Kai-Chi Chen	11844-US-PA	1685

31561 7590 09/23/2005

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER
THAI, LUAN C

ART UNIT	PAPER NUMBER
2891	

DATE MAILED: 09/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/707,686	CHEN ET AL.	
	Examiner	Art Unit	
	Luan Thai	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office action is responsive to the amendment filed July 26, 2005.

Claims **1-22** are pending in this application.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-3, 5-7, and 9 are rejected under 35 U.S.C. 102(e) as being anticipated by Huang et al. (6,538,321).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 1, 2, 5, 6, 9, Huang et al. (see specifically figures 5 and 8) disclose a chip package structure, comprising: a packaging substrate (1), a chip (2) electrically connected to the carrier (1) in a flip-chip bonding process (e.g., via solder bump 3a), a heat sink (10), set over the chip, wherein the heat sink has a surface area greater than the chip and is unconnected to the carrier (1); an encapsulating material layer (5) of resin formed in a simultaneous molding process (see figure 4, Col. 3, lines 29+) to cover the chip, the heat sink and the carrier, wherein the heat

sink (10) having standoff components (11) set over the heat sink such that a height of the standoff component above the heat sink is equal to the thickness of the encapsulating material (5) over the heat sink, and wherein a top surface of the encapsulating material is higher than that of the heat sink portion (10).

Regarding claim 3, the chip package structure of Huang et al. further comprises a thermal conductive adhesive layer (6) set between the top surface of the chip and the heat sink.

Regarding claims 7, wherein the package further comprises an array of solder balls (7) attached to a carrier surface away from the chip.

3. Claims 1-3, 5-7 and 9 are rejected under 35 U.S.C. 102(e) as being anticipated by Combs et al. (6,734,552).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 1, 2, 5, 6, 9, Combs et al. (see specifically figures 1-5) disclose a chip package structure, comprising: a packaging substrate (100), a chip (130) electrically connected to the carrier (100) in a flip-chip bonding process (e.g., via solder bump 105), a heat sink (110), set over the chip, wherein the heat sink has a surface area greater than the chip and is unconnected to the carrier (100); an encapsulating material layer (140) of resin formed in a simultaneous molding process (see figure 2) filling a bonding gap between the chip and the carrier and covering the heat sink and the carrier, wherein the heat sink (110) having standoff component (112) set over the heat sink such that a height of the standoff component above the heat sink is

equal to the thickness of the encapsulating material (140) over the heat sink, and wherein a top surface of the encapsulating material is higher than that of the heat sink portion (114).

Regarding claim 3, the chip package structure of Combs et al. further comprises a thermal conductive adhesive layer (119) set between the top surface of the chip and the heat sink.

Regarding claims 7, wherein the package further comprises an array of solder balls (106) attached to a carrier surface away from the chip.

4. Claims 1, 5-7, and 9 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamada et al. (6,476,502).

The figures and reference numbers referred to in this office action are used merely to indicate an example of a specific teaching and are not to be taken as limiting.

Regarding claims 1, 5-7, and 9, Yamada et al. (see specifically figure 9) disclose a chip package structure, comprising: a packaging substrate (12), a chip (16) electrically connected to the carrier (12) in a flip-chip bonding process (e.g., via solder bump 32), a heat sink (62), set over the chip (16), wherein the heat sink has a surface area greater than the chip and is unconnected to the carrier (12); an encapsulating material (10/24) of resin formed in a simultaneous molding process (Col. 3, lines 25+) filling a bonding gap between the chip and the carrier and covering the heat sink and the carrier, wherein a top surface of the encapsulating material is higher than that of the heat sink (62).

5. Claims 1-3, 5-12, 14-15, and 18-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Ference et al. (6,265,771).

Regarding claims 1-3, 5-12, 14-15, and 18-22, Ference et al. (see specifically figures 2 and 4) disclose a chip package structure, comprising: a packaging substrate (42c), a chipset

comprising a first chip (12), having a first active surface, wherein the first chip is attached to the carrier (42c) such that the first active surface is positioned away from the carrier (42c), and a second chip (16), having a second active surface with a plurality of bumps (18) thereon, wherein the second active surface of the second chip (16) is bonded and electrically connected to the first chip (12) in a flip-chip bonding process such that the bumps between the second chip (16) and the first chip (12) set up a flip-chip bonding gap, and wherein the chipset further comprises a plurality of conductive wires (28) with ends connected electrically to the first chip (12) and the carrier (42c) respectively. Ference et al. further disclose a heat sink (26) of metal having a surface area greater than chip (16) and bonded to the chip (16) via a thermal conductive adhesive layer (Col. 3, lines44+), an encapsulating material of resin (54) formed in a simultaneous molding process (Col. 12, lines 50+) to cover the chipset, the heat sink and the carrier. Hoffman et al. further disclose an array of solder balls (48) attached to a carrier surface away from the chipset, wherein the heat sink (26) having standoff component (see figures 2 and 4) set over the heat sink such that a height of the standoff component above the heat sink is equal to the thickness of the encapsulating material (54) over the heat sink, and wherein a top surface of the encapsulating material is higher than that of the heat sink portion around the standoff component, and wherein the package further comprises a passive component electrically connected to the carrier (Col. 2, lines 40+, Col. 3, lines 48+).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a

whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 4 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ference et al. (6,265,771) in view of Nishioka et al. (JP-02000195994A of record).

In regard to claim 4, Ference et al. disclose the claimed limitations as mentioned above except for specifying the thermal conductivity of the encapsulating material to be greater than 1.2W/m.K.

Nishioka et al. while related to a similar encapsulating material design teach that a sealing resin composition having a thermal conductivity not smaller than 4.0 W/m.K is used as an encapsulating material to improve heat conductivity and flame resistance (see the Abstract). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the encapsulating material having a thermal conductivity not smaller than 4.0 W/m.K, as taught by Nishioka et al., to Ference et al.'s package structure in order to improve heat conductivity and flame resistance of the semiconductor device.

8. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Combs et al. (6,734,552) in view of Nishioka et al. (JP-02000195994A of record).

In regard to claim 4, Combs et al. disclose the claimed limitations as mentioned above except for specifying the thermal conductivity of the encapsulating material to be greater than 1.2W/m.K.

Nishioka et al. while related to a similar encapsulating material design teach that a sealing resin composition having a thermal conductivity not smaller than 4.0 W/m.K is used as an encapsulating material to improve heat conductivity and flame resistance (see

the Abstract). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the encapsulating material having a thermal conductivity not smaller than 4.0 W/m.K, as taught by Nishioka et al., to Combs et al.'s package structure in order to improve heat conductivity and flame resistance of the semiconductor device.

9. Claims 10 and 16-17 are rejected under 335 U.S.C. 103(a) as being unpatentable over Hoffman et al. (6,737,750) in view of Combs et al. (6,734,552).

Regarding claims 10 and 16-17, Hoffman et al. (see specifically figures 12a and 13) disclose a chip package structure, comprising: a packaging substrate (10), a chipset set over and electrically connected to the carrier (10), wherein the chipset comprises: a first chip (12) having an active surface with a plurality of first bumps thereon, wherein the first active surface of the first chip is bonded and electrically connected to the carrier in a flip-chip bonding process such that the first bumps between the first chip and the carrier set up a flip-chip bonding gap; a second chip (16) having a second active surface, wherein the second chip is attached to the first chip (12) such that the second active surface is positioned away from the first chip, wherein a plurality of conductive wires (20a) with ends electrically connected to the second chip (16) and the carrier (10) respectively; and a third chip (Col. 11, lines 40+) having a third active surface with a plurality of second bumps thereon, wherein the third active surface of the third chip is bonded and electrically connected to the second chip (16) in a flip-chip bonding process. Hoffman et al. further disclose an encapsulating material of resin (19) formed in a simultaneous molding process (Col. 12, lines 50+) to cover the chips, the heat sink and the carrier, and an array of solder balls (15) attached to a carrier (10) surface away from the chipset. Hoffman et al. do not explicitly teach a heat sink set over the chipset (e.g., over the third chip) having a surface area

grater than the chipset, being unconnected to the carrier, and the top surface being lower than the top surface of the encapsulant material.

Combs et al. while related to a similar dissipation integrated circuit package design teach (see specifically figures 3-7) a heat sink (110) set over the chip (130), wherein the heat sink (110) has a surface area grater than the chip (130), being unconnected to the carrier (100), and wherein the top surface of the encapsulant material (140) is higher than that of the heat sink (110), in order to dissipate the heat from the integrated circuit package in an efficient manner (Col. 1, lines 15+). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that modifying Hoffman et al.'s package by attaching the heat sink structure, as disclosed by Combs et al, to the third chip would have been beneficial because such heat sink helps dissipating the heat from the integrated circuit package in an efficient manner.

Conclusion

10. Applicant's arguments with respect to claims **1-22** have been fully considered, but they are deemed to be moot in view of the new grounds of rejection.

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action because the newly added limitations (e.g., the underlined portions) in independent claims 1 and 10 raise new issues that would require further consideration and/or search. Accordingly, THIS ACTION IS MADE FINAL. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luan Thai whose telephone number is 571-272-1935. The examiner can normally be reached on 6:30 AM - 5:00 PM, Monday to Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bradley W. Baumeister can be reached on 571-272-1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Luan Thai
Primary Examiner
Art Unit 2891
September 20, 2005